REMARKS

Claims 1-40 were pending in the application (erroneously numbered as 1-39). By this paper, Applicant has amended Claims 1-4, 6-8, 11-12, 14, 19-21, 25, 28-32, and 36-40, and added new Claims 41-43. Hence, Claims 1- 43 are presented for examination herein.

Request For Supervisory Interview and Review

For reasons set forth below, Applicant hereby respectfully and formally requests a personal and/or telephonic interview between the Applicant (including the inventor, Dr. Eric M. Dowling) and the Examiner's Supervisor regarding the instant application, as well as two closely related applications (U.S. Serial No. 10/074,779 filed February 13, 2002, and Serial No. 10/001, 007 filed November 14, 2001). Applicant requests that such interview(s) be conducted at the earliest opportunity convenient to the Examiner's Supervisor.

Applicant further formally requests the Examiner's Supervisor to become substantively involved in the details of this examination, and perform a detailed review Office Actions in this application from this point forward. Applicant respectfully submits that many claims as previously presented clearly defined allowable subject matter over the art of record, yet were summarily rejected on what Applicant believes are highly specious legal and technical bases.

Applicant specifically herein reserves the right to appeal to the board of Administrative Patent Judges.

Amendments to the Title

In response to Par. 3 of the Office Action, Applicant respectfully traverses the Examiner's assertion that the previously presented title lacks descriptiveness. The term "Embedded-DRAM-DSP Architecture" is completely descriptive of the broadest generic embodiment of the invention. Requiring Applicant to further include specific attributes or limitations from its claims is an unnecessary restriction on Applicant's right to claim its invention broadly; such additional limitations in the title potentially affecting the claim scope afforded to Applicant.

It is well settled precedent that a patentee is in no way limited to specific embodiments set forth in its specification, and Applicant submits that the inclusion of further aspects of certain

embodiments of its invention as requested by the Examiner violates the foregoing well-settled principle.

However, by this paper, Applicant has amended the title of the Application to be as descriptive as possible without unduly limiting or affecting the genericism of the title (and hence potentially the claims).

Amendments to the Specification

By this paper, Applicant has amended the Abstract of the Invention in order to more clearly set forth the invention, and to comply with the 150-word limit.

Pursuant to Pars. 5-7 of the Office Action, Applicant has herein amended various portions of the specification in order to correct the reference numeral deficiencies cited by the Examiner. No new matter has been added by these amendments.

Amendments to the Drawings

Also pursuant to Pars. 5-7 of the Office Action, Applicant has herein amended Figs. 2 and 4 of the specification in order to correct the remaining reference numeral deficiencies cited by the Examiner not addressed by amendment of the specification. No new matter has been added by these amendments.

Claims Objections

Per Pars. 8-18 of the Office Action, Claims 35-39 were objected to as being numbered incorrectly, and Claims 8, 11, 12, 20, 25, 28, 29, 36, and 40 were objected to for various informalities. Per this response, Applicant has renumbered Claims 35-39 as Claims 36-40, and corrected the various informalities cited by the Examiner. Applicant submits that these amendments overcome the Examiner's objections.

Rejections under 35 U.S.C. §112

Per Pars. 19-26 of the Office Action, Claims 4, 6-7, 12 and 30-31 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as his invention.

By this paper, each of the foregoing claims has been amended accordingly, and Applicant submits that all such rejections under 35 U.S.C. § 112 have been overcome.

Rejections under 35 U.S.C. §103

In response to the Examiner Section 103 Rejections of Claims 1-40 (previously numbered 1-39) as set forth in Pars. 27-73 of the Office Action, Applicant provides the following.

1) Traversal of All "Official Notice"

By this paper, Applicant traverses all explicit and implicit "Official Notice" taken by the Examiner in the Office Action per, *inter alia*, MPEP 2144.03C, and requests the Examiner to present documentary evidence of the prior art on which to base his obviousness rejections, or to withdraw all such improper rejections currently standing in this application.

(i) **Non-judicious use of Official Notice** - MPEP 2144.03 states in relevant part:

> *"In limited circumstances, it is appropriate for an examiner to take official notice of facts not in the record or to rely on "common knowledge" in making a rejection, however such rejections should be judiciously applied.*
> ...
> *The standard of review applied to findings of fact is the "substantial evidence" standard under the Administrative Procedure Act (APA). See In re Gartside, 203 F.3d 1305, 1315, 53 USPQ2d 1769, 1775 (Fed. Cir. 2000). See also MPEP § 1216.01.*
> ...
> *While "official notice" may be relied on, these circumstances should be rare when an application is under final rejection or action under 37 CFR 1.113. Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known. As noted by the court in In re Ahlert, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970), the notice of facts beyond the record which may be taken by the examiner must be "**capable of such instant and unquestionable demonstration as to defy dispute**" (citing In re Knapp Monarch Co., 296 F.2d 230, 132 USPQ 6 (CCPA 1961)).*" {Emphasis added}

The Examiner has explicitly utilized "Official Notice" as a basis of rejection in no less than nineteen (19) separate instances within the Office Action (**including at least once in each of fourteen (14) independent claims presented, thereby causing Official Notice to be a substantive basis of all rejections of all claims, dependent and independent, previously presented**), and further has implicitly used Official Notice in numerous other instances (e.g.,

using the word "inherent" and variations thereof). Applicant submits that this cannot in any way be considered "judicious application" in "limited circumstances" as required by the MPEP.

Applicant notes for example that the Examiner has utilized two Official Notices in concocting his basis for rejection of each of independent Claims 14, 19 and 33; hardly a judicious use in limited circumstances.

Hence, the Examiner's repeated and excessive use of Official Notice in all forms (i.e., explicit and implicit) immediately renders his obviousness rejections suspect on, *inter alia*, both procedural and substantive grounds.

(ii) **Improper Use of "Official Notice" as Principal Evidence of Obviousness** – In addition to the foregoing, the Examiner improperly uses such explicit or implicit Official Notice as a critical or principal basis of all of his rejections of the independent claims. Such Official Notice is improper and clearly not in accordance with MPEP 2144.03A&B; *"It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. Zurko,* 258 F.3d at 1385, 59 USPQ2d at 1697 {emphasis added}. See, e.g., the discussion of Claims 14, 19, and 33 below for but one example of how such Official Notice is improperly used as a principal basis of rejection in the Office Action.

Also, as previously noted, Official Notice comprises the basis for rejection of every one of 14 independent claims in the application. It stretches credibility beyond all bounds to say that none of these uses comprises a "principal" basis for rejection as proscribed by MPEP 2144.03A&B. See especially Claims 14, 19, and 33, wherein **two** explicit Official Notices and only **one** prior art reference are used as the basis of rejection.

Furthermore, the Examiner's repeated citation of Official Notice throughout the Action for the proposition that "DRAM and its advantages are well known and expected in the art" (see, e.g., Par. 59, regarding Claim 19) comprises an improper use of Official Notice pursuant to MPEP 2144.03A-C. Applicant's invention of, e.g., Claim 19 utilizes a specific optimized architecture including an embedded DRAM processor that interfaces directly to DRAM.

The Examiner's use of Official Notice in this instance is akin to asserting that a hypothetical claimed monoplane (single wing aircraft) is obvious over (i) bi-plane prior art, combined with (ii) Official Notice that "use of a wing" is well known. Clearly, the invention of

the monoplane required additional inventive novelty and inventive step over the bi-plane prior art. The entire architecture of the claimed monoplane (e.g., wings, fuselage, landing gear, etc.) is adapted specifically for a craft with a **single** set of wings. Hence, the Official Notice of "a wing" is improperly used as the primary basis of the rejection, being "boot-strapped" to the bi-plane art to ostensibly teach or suggest something which it clearly does not (i.e., an aircraft with a single set of wings capable of flying).

In the present context (exemplary Claim 19), the Examiner's Official Notice that "DRAM and its advantages are well known and expected in the art" is being boot-strapped onto Parady (US 5,933,627), which teaches nothing of DRAM, to ostensibly form Applicant's claimed invention, thereby improperly using such Official Notice as the primary basis for rejection. Stated differently, without this Official Notice, the Examiner's obviousness arguments fall apart, since Parady does not teach anything to do with DRAM.

Per MPEP 2144.03C, Applicant hereby requests that the Examiner provide explicit references that teach an embedded DRAM processor with the functionality of the claimed inventions, since the Examiner has failed to do so to this point.

(iii) **Improper Standards Applied in Use of "Official Notice"** – Yet in addition to the foregoing, Applicant submits that the Examiner has utilized an improper standard in all instances of his Official Notice; i.e., the "facts" that the Examiner cites as being well known are clearly related to the state of the art and subject to argument. MPEP 2144.03A states:

> *"It would **not** be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must **always** be supported by citation to some reference work recognized as standard in the pertinent art. In re Ahlert, 424 F.2d at 1091, 165 USPQ at 420-21. See also In re Grose, 592 F.2d 1161, 1167-68, 201 USPQ 57, 63 (CCPA 1979) ... In re Eynde, 480 F.2d 1364, 1370, 178 USPQ 470, 474 (CCPA 1973) ("[W]e reject the notion that judicial or administrative notice may be taken of the state of the art. The facts constituting the **state of the art** are normally subject to the possibility of rational disagreement among reasonable men and are **not** amenable to the taking of such notice.")."* {Emphasis added}

A most illuminating example on this point is the Examiner application of Official Notice to those of Applicant's claims discussing generally data movement operations that interfaces directly to DRAM, (e.g., performing data move operations on the cache-DRAM type register file prior to switching the cache-DRAM type register file into an architectural register set). In this specific context, it is clearly improper to use Official Notice to support a blanket rejection of "register-register move operations are well known and expected...."; see e.g., Par. 29 of the Office Action relating to Claim 1. Applicant agrees that data move operations generically are well known, but not in the context of Applicant's invention of Claim 1; i.e., an embedded DRAM processor that interfaces directly to DRAM. Per MPEP 2144.03C, **Applicant hereby requests that the Examiner provide explicit references that teach such functionality in the context of an embedded DRAM processor, since the Examiner has failed to do so to this point.**

Based on items (i)-(iii) above, Applicant submits that the Examiner has improperly utilized all instances of Official Notice in rejecting, *inter alia*, Claims 1, 2, 3, 4, 6, 7, 11, 12, 14, 19, 21, 29, 33 and 40 (as well as their dependent Claims), and that all such rejections predicated on "Official Notice" (whether explicit or implicit) must be withdrawn.

2) Characterization and Use of the Prior Art

The Examiner is respectfully reminded that proper patent examinations and proper rejections must rely on the written record of the prior art, not subjective opinion or determination.

When prior art is used, the prior art must be properly characterized and taken in proper context, and only combined when there is a proper reason or motivation to combine (see MPEP 2143). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Prior art that teaches away from the invention under Examination cannot be relied upon merely because it happens to contain a stray word relative to an element of the claimed invention.

Applicant respectfully submits that the Examiner has significantly mischaracterized several pieces of prior art to fashion his rejections, which clearly contravenes proper examination procedure. Such mischaracterizations are described below.

3) Distinctions Over the Prior Art

(i) Per Par. 28 of the Office Action, Claims 1, 24, 27, and 35-36 were rejected under Section 103(a) over Parady (US 5,933,627) in view of Inagami (US 4,881,168), as well as "Official Notice".

Claim 1 – By this paper, Applicant has amended Claim 1 to include limitations relating to said first portion of said architecture, at a given time, seeing a first subset of the total available registers as its set of architectural registers while a second subset of the total available registers is not accessible by the first portion of the architecture. Applicant submits that none of the cited art, including Parady and Inagami, teach or suggest such functionality.

The Examiner's reasoning regarding Claim 1 is fallacious. Suppose in Paraday (as the Examiner suggests), the claimed "first portion" corresponds to Parady's floating point hardware 38, 40. Suppose also (as the Examiner suggests) that the claimed "second portion" of the architecture corresponds to Parady's load/store unit 32. Given this mapping, Parady clearly teaches away from the invention of Claim 1 because in Parady, the load/store unit can only access the architectural registers, and cannot access any of the deactivated register sets.

Note further that Parady assumes a cache is between the load/store unit 32 and any memory that might be there. Therefore, the load/store unit 32 cannot rightfully be called the "data assembly unit" as it is alleged by the Examiner on, *inter alia*, page 8, Par. 29.c). "*If the proposed modification or combination of the prior art would change the* ***principle of operation*** *of the prior art invention being modified, then the teachings of the references are* ***not*** *sufficient to render the claims prima facie obvious.*" MPEP 2143.01 {emphasis added}

The Examiner also states on page 9, Par. 29.f) of the Office Action:

> *"Parady has not taught ...a set of selected elements of a row of said DRAM array into a selected set of data registers,...However, Inagami has taught performing such operations."* {Emphasis added}

Applicant request the Examiner to reconcile this with his statements on, *inter alia*, page 14, subparagraph e):

> *"Inagami has not explicitly taught that the memory array is a DRAM array."* {Emphasis added}

Applicant can only conclude from this inconsistency that the Examiner is again utilizing Official Notice (here, a second instance of Official Notice asserted as a basis of rejecting Claim 1; see below). Neither Parady nor Inagami teach or suggest an embedded DRAM processor nor a method of intelligent caching for such a processor. Applicant traverses the Examiner's implicit use of "Official Notice" that the use of DRAM would be obvious, because the invention of Claim 1 is specifically designed to provide an intelligent caching interface to slower DRAM, and **none** of the cited prior art addresses the problem of improving performance of a processor that interfaces directly to DRAM without a need for a caching system.

Applicant further traverses the Examiner's explicit Official Notice (regarding register-register move operations). The prior art presented by the Examiner in no way teaches or suggests a register move unit that allows data to be arranged in an inactive register file while other functional units operate on activated architectural registers. **Applicant requests pursuant to MPEP 2144.03C that the Examiner provide explicit documentation to this effect.**

Accordingly, Applicant submits that the invention of Claim 1 is novel and non-obvious over the cited art, and in condition for allowance.

(ii) Per Par. 33 of the Office Action, Claim 2 was rejected under Section 103(a) over Hayashi (5,237,702) in view of Jager (US 5,423,048), as well as "Official Notice". Applicant provides the following remarks.

Claim 2 – By this paper, Applicant has amended Claim 2 to include limitations relating to the recited main memory being implemented as one or more banks of DRAM without a caching system that employs cache hits and cache misses. Support for this limitation is replete throughout Applicant's specification including, *inter alia*, on page 6, lines 9-21.

The claim language has also been clarified to indicate that instructions are dispatched to the first and second portions in parallel; Hayashi teaches a single instruction stream, some of the instructions being load/store instructions and some being arithmetic instructions.

Yet further clarification of Claim 2 provided herein relates to the intelligent caching system obviating the need for a multilevel caching system as used in the prior art to interface with DRAM.

The claim language has still further been clarified to show that the prefetching is of data and not instructions (see discussion regarding combination of Jager and Hayashi below).

Hayashi teaches away from the concept of intelligent caching as set forth in Claim 2. The Examiner is directed to, *inter alia*, the Hayashi abstract, Fig. 2-5, and Claim 1 thereof. See also Col. 2, lines 3-30. Applicant has carefully analyzed Hayashi and finds that the vector processor executes a single sequential instruction stream. **There is simply no teaching or suggestion in Hayashi of a first portion of an architecture performing speculative data preloads for a second portion of the architecture that executes separate instructions.** Instead, Hayashi teaches a contention management scheme to load registers prior to the issuance of a subsequent vector calculation command. The entire Hayashi solution is directed at managing contentions, busy conditions and the amount of waiting time related to calculations, which are problems that are completely obviated by performing parallel prefetching and intelligent caching as per the Applicant's invention of Claim 2. Stated differently, Hayashi is effective at dealing with the details of problems completely avoided by the Applicant's invention, and hence would lead one of ordinary skill away from the claimed invention.

For example, Hayashi teaches at Col. 4, lines 8-38:

> *"As shown in FIG. 4, resource manager 14 essentially comprises load wait management flags 300, load busy management flags 301, read busy management flags 302, and write busy management flags 303. (...) Specifically, load wait management flags 300 are set in response to a proceed-to-transfer signal from the contention detector 13 and reset in response to a start-of-transfer signal from the memory controller 2. (...) A time management circuit 304 is provided to receive from the stack 12 a count of vector elements contained in each instruction and determines the amount of time elapsed from the reception of a proceed-to-calculate instruction to the time at which the reading of a given vector register is complete and further determines the amount of time elapsed from the reception of the proceed-to-calculate instruction to the time at which the writing of the given vector register is complete."* {Emphasis added}

As can be seen, Hayashi teaches away from the present invention, as one of ordinary skill in the art following Hayashi would seek ways to address contentions and to minimize delays associated therewith, instead of generating a fundamentally different concept of operation to avoid these problems altogether.

As to Jagger, there would be no reason to combine Jagger with Hayashi to arrive at the present invention. Jagger teaches a speculative prefetch method for prefetching instructions, as opposed to data to be used as operands for instructions (and operated on as operands) as in Applicant's invention; see e.g., page 26, line 22 to page 27, line 4 of the specification as filed.

Accordingly, Applicant submits that the invention of Claim 1 is novel and non-obvious over the cited art, and in condition for allowance.

(iii) Per Par. 35 of the Office Action, Claim 3 was rejected under Section 103(a) over Inagami (US 4,881,168), in view of Hayashi (US 5,933,627) and Jager, as well as "Official Notice". Applicant provides the following remarks.

Claim 3 – By this paper, Applicant has amended Claim 3 to include numerous additional limitations yet further distinguishing the claimed invention over the cited art, including *inter alia*, limitations relating to dispatching in parallel a first sequence of instructions and a second sequence of instructions. As acknowledged by the Examiner on page 13 (Par. 36.c) of the Action, Inagami does not teach a second sequence of instructions. Furthermore, as noted previously herein with respect to Claim 2, Hayashi teaches only a single instruction stream. Jager similarly does not these limitations.

Hence, Applicant submits that Claim 3 as presented herein clearly distinguishes over these references, since they cannot be combined to produce Applicant's invention.

(iv) Per Par. 37 of the Office Action, Claims 4, 12, 20, and 29-32 were rejected under Section 103(a) over Parady in view of Bissett (US 5,896,523), as well as "Official Notice". Applicant provides the following remarks.

Claim 4 – By this paper, Applicant has amended Claim 4 to add limitations relating to dispatching in parallel the first sequence of instructions and a second sequence of instructions. Support for this amendment is replete throughout the specification, including *inter alia* page 13, lines 4-9. As previously noted, none of the cited art teaches or suggests such functionality.

Claim 4 further already includes the limitations relating to active and inactive register sets, and loading the inactive set. Parady clearly *teaches away* from the invention of Claim 4 because in Parady, the load/store unit can only access the architectural registers, and cannot access any of the deactivated register sets. The active thread completely controls the functional units and the load/store units.

Furthermore, nowhere does Bissett discuss performing data prefetches in the background even remotely resembling those taught by Applicant, as asserted by the Examiner on page 16 of the Action. See Col. 3, line 25 to Col. 4, line 8 of Bissett:

> *"The invention provides techniques for maintaining synchronized execution of loosely-coupled processors of a fault tolerant or fault resilient computer system. The processors operate in lockstep with respect to a quantum of instructions, referred to as quantum synchronization, but operate independently with respect to individual instructions. For example, the processors may be Intel Pentium Pro processors executing the Microsoft Windows NT operating system. (...) In general, the processors operating in quantum synchronization with each other are referred to as compute elements. A compute element is defined as a redundant processing engine for which sources of asynchrony have been removed by any of a number of software and hardware techniques. For a processor to constitute a viable compute element, all software-perceivable system activities that are random or asynchronous in nature must be removed, disabled, or made synchronous. For example, any input/output activity which could affect the software execution path of the processor must be eliminated or handled in some instruction-synchronous fashion. (...) Some asynchronous processor-related operations do not influence software execution, and need not be disabled or otherwise addressed. Examples of such operations include background DMA, memory refresh, cache fills and writebacks, branch prediction, instruction prefetch, and data prefetch."* {Emphasis added}

Bissett only mentions "data prefetch" four times, twice in the claims and twice in the specification, and always in the context of allowable asynchronous operations in a quasi-synchronous parallel processing system. Instead of teaching or suggesting the Applicant's invention wherein different portions of an architecture work in harmony, one preparing data for (and in advance of) the needs of the other portion(s), Bissett teaches a system where all parallel processors execute the exact same sequence of instructions and operate in a quasi-lock-step. That is, each processor executes the same set of instructions, but not in instruction-level lock step, yet then resynchronize at synchronization points.

Also, each instruction-executing processor is a separate processor (e.g., a Pentium) as opposed to a portion of a single cooperative processor architecture as per Applicant's invention. Hence Applicant submits that Bissett has been mischaracterized, and in fact teaches away from the Applicant's invention on multiple accounts.

Hence, Applicant submits that Claim 4 as presented herein clearly distinguishes over these references, since they cannot be combined to produce Applicant's invention.

Claim 12 – Applicant traverses the Examiner's Section 103 rejection of Claim 12 in its entirety. Note that Parady assumes a cache is between the load/store unit 32 and any memory that might be utilized. Therefore the load/store unit 32 cannot rightfully be called the data assembly unit.

Furthermore, as discussed above with respect to Claim 4, Applicant submits that Examiner has significantly mischaracterized Bissett as teaching "data prefetches in the background"(see Par. 39, top of page 18 of the Action regarding Claim 12). Bissett does not teach such prefetches, but rather a system where all parallel processors execute the exact same sequence of instructions and operate in a quasi-lock-step.

Hence, Applicant submits that Claim 12 as presented herein clearly distinguishes over these references, since they cannot be combined to produce Applicant's invention.

Claim 29 – Applicant herein traverses the Examiner's Section 103 rejection of Claim 29 in its entirety. Note that Parady's load/store unit (i) can only interact with active registers, (ii) is coupled to L2 and L2 cache (not DRAM), (iii) and performs thread switches when the caching system causes an L2 miss. The load/store unit of Parady cannot in any way be compared to the claimed invention.

Furthermore, as discussed above with respect to Claim 4, Applicant submits that Examiner has significantly mischaracterized Bissett as teaching "data prefetches in the background"(see middle of page 21 of the Action regarding Claim 29). Bissett does not teach such prefetches, but rather a system where all parallel processors execute the exact same sequence of instructions and operate in a quasi-lock-step.

Hence, Applicant submits that Claim 29 as presented herein clearly distinguishes over these references, since they cannot be combined to produce Applicant's invention.

(v) Per Par. 45 of the Office Action, Claims 5, 7-10 and 13 were rejected under Section 103(a) over Parady in view of Bissett, and further in view of Jager, as well as "Official Notice". Applicant provides the following remarks.

Claim 7 – By this paper, Applicant has amended Claim 7 to clarify that the recited splitting of a single program comprises splitting into first and second parallely dispatched and executed portions. Support for this amendment is found at, *inter alia*, page 12, lines 10-26 of the specification as filed. None of the cited art teaches or suggests such limitations in combination with the other elements of Claim 7.

Furthermore, as discussed above with respect to Claim 4, Applicant submits that Examiner has significantly mischaracterized Bissett as teaching "data prefetches in the background"(see Par. 39, top of page 18 of the Action regarding Claim 12). Bissett does not teach such prefetches, but rather a system where all parallel processors execute the exact same sequence of instructions and operate in a quasi-lock-step.

Hence, Applicant submits that Claim 7 as presented herein clearly distinguishes over the cited art on multiple bases.

(vi) Per Par. 52 of the Office Action, Claims 6, 14-19, 21-23, 25-26, 28, 33-34 and 37-40 were rejected under Section 103(a) over Parady, as well as "Official Notice". Applicant provides the following remarks.

Claim 6 – Applicant herein traverses the Examiner's Section 103 rejection of Claim 6 in its entirety, as well as the Examiner's Official Notice (both).

Note that Parady assumes a cache is between the load/store unit 32 and any memory that might be there. Therefore, the load/store unit 32 cannot rightfully be called the "data assembly unit" as it is alleged by the Examiner on, *inter alia*, page 28, Par. 53). "*If the proposed modification or combination of the prior art would change the* ***principle of operation*** *of the prior art invention being modified, then the teachings of the references are* ***not*** *sufficient to render the claims prima facie obvious.*" MPEP 2143.01 {emphasis added}. Parady teaches away from the claimed invention in at least this regard.

Parady in no way teaches or suggests an embedded DRAM processor nor a method of intelligent caching for such a processor. Applicant traverses the Examiner's use of "Official Notice" that the use of DRAM would be obvious, because the invention of Claim 6 is specifically designed to provide an intelligent caching interface to slower DRAM.

Applicant further traverses the Examiner's explicit Official Notice (regarding at least one row of said DRAM array to be speculatively prefetched). The prior art presented by the Examiner in no way teaches or suggests speculative prefetch of a row of DRAM, let alone a non-speculative one. **Applicant requests pursuant to MPEP 2144.03C that the Examiner provide explicit documentation to this effect.**

Accordingly, Applicant submits that the invention of Claim 6 is novel and non-obvious over the cited art, and in condition for allowance.

Claim 14 - Applicant herein traverses the Examiner's Section 103 rejection of Claim 14 in its entirety, as well as the Examiner's Official Notice (both).

The Examiner basically attempts to say that "prefetching is known", and "precharging is inherent in DRAM", and therefore "it would be obvious to modify Parady to include a speculative prefetch including precharge of DRAM." Aside from the fact that Parady (as well as the other art cited) admittedly does not teach DRAM (see first Official Notice of two used to reject this Claim), it is nonsensical to then assert that such an approach would be combinable with Parady's architecture, let alone suggested or motivated. Note that Parady's load/store unit can only interact with active registers, and is coupled to L2 and L2 cache (not DRAM). This teaches away on multiple bases from a data assembly unit that speculatively fetches one or more rows of DRAM into a register file, along with the other limitations as set forth in Applicant's Claim 14.

Furthermore, in Parady there is no intelligent caching program as set forth by Applicant, but instead there is ordinary caching that causes thread switches in response to long L2 cache delays caused by a particular thread.

Applicant respectfully submits that Claim 14 is but another example of where the Examiner's application of "Official Notice" exceeds all guidance provided by the MPEP, specifically in that two separate Notices are used to reject the same claim, with only one actual

prior art reference, and such Notice clearly acts as a primary basis for rejection in contravention of MPEP 2144.03A&B discussed previously herein.

Accordingly, Applicant submits that the invention of Claim 14 is novel and non-obvious over the cited art, and in condition for allowance.

Claim 19 – Applicant traverses the Examiner's Section 103 rejections of Claim 19 in their entirety.

Note that Parady assumes a cache is between the load/store unit 32 and any memory that might be there. Therefore, the load/store unit 32 cannot rightfully be called the "data assembly unit" as it is alleged by the Examiner on, *inter alia*, page 33, Par. 59.c). "*If the proposed modification or combination of the prior art would change the **principle of operation** of the prior art invention being modified, then the teachings of the references are **not** sufficient to render the claims prima facie obvious.*" MPEP 2143.01 {emphasis added}. Parady teaches away from the claimed invention in at least this regard.

Parady in no way teaches or suggests an embedded DRAM processor nor a method of intelligent caching for such a processor. Applicant traverses the Examiner's use of "Official Notice" that the use of DRAM would be obvious, because the invention of Claim 19 is specifically designed to provide an intelligent caching interface to slower DRAM.

Applicant further traverses the Examiner's explicit Official Notice (regarding at least one row of said DRAM array to be speculatively prefetched). The prior art presented by the Examiner in no way teaches or suggests speculative prefetch of a row of DRAM, let alone a non-speculative one. **Applicant requests pursuant to MPEP 2144.03C that the Examiner provide explicit documentation to this effect.**

Again, the Examiner's application of "Official Notice" exceeds all guidance provided by the MPEP, specifically in that two separate Notices (and only one actual prior art reference) are used to reject the same claim, and clearly acts as a primary basis for rejection in contravention of MPEP 2144.03A&B discussed previously herein.

Accordingly, Applicant submits that the invention of Claim 19 is novel and non-obvious over the cited art, and in condition for allowance.

Claim 21- Applicant traverses the Examiner's Section 103 rejections of Claim 21 in their entirety.

Note that Parady assumes a cache is between the load/store unit 32 and any memory that might be there. Applicant notes that Parady is designed to cause thread switches in response to long delays caused by L2 cache hits. The load/store unit of Parady is coupled through two layers of cache as opposed to being coupled to DRAM. Therefore, the load/store unit 32 cannot rightfully be called the "data assembly unit" as it is alleged by the Examiner on, *inter alia*, page 34, Par. 60.c). "*If the proposed modification or combination of the prior art would change the **principle of operation** of the prior art invention being modified, then the teachings of the references are **not** sufficient to render the claims prima facie obvious.*" MPEP 2143.01 {emphasis added}. Parady teaches away from the claimed invention in at least this regard.

Furthermore, Parady in no way teaches or suggests an embedded DRAM processor nor a method of intelligent caching for such a processor. Applicant traverses the Examiner's use of "Official Notice" that the use of DRAM would be obvious, because the invention of Claim 21 is specifically designed to provide an intelligent caching interface to slower DRAM.

Accordingly, Applicant submits that the invention of Claim 21 is novel and non-obvious over the cited art, and in condition for allowance.

Claim 33 - Applicant traverses the Examiner's Section 103 rejections of Claim 33 in their entirety.

Note that Parady assumes a cache is between the load/store unit 32 and any memory that might be there. Therefore, the load/store unit 32 cannot rightfully be called part of the "data assembly unit" as it is alleged by the Examiner on, *inter alia*, page 37, Par. 66.b). "*If the proposed modification or combination of the prior art would change the **principle of operation** of the prior art invention being modified, then the teachings of the references are **not** sufficient to render the claims prima facie obvious.*" MPEP 2143.01 {emphasis added}. Parady teaches away from the claimed invention in at least this regard.

Parady in no way teaches or suggests an embedded DRAM processor nor a method of intelligent caching for such a processor. Applicant traverses the Examiner's use of "Official Notice" that the use of DRAM would be obvious, because the invention of Claim 33 is specifically designed to provide an intelligent caching interface to slower DRAM.

Applicant further traverses the Examiner's explicit Official Notice (regarding at least one row of said DRAM array to be speculatively prefetched or loaded in parallel). The prior art cited by the Examiner in no way teaches or suggests speculative prefetch of a row of DRAM, let alone a non-speculative one. It further does not teach loading in parallel. **Applicant requests pursuant to MPEP 2144.03C that the Examiner provide explicit documentation to this effect.**

Again, the Examiner's application of "Official Notice" exceeds all guidance provided by the MPEP, specifically in that two separate Notices are used to reject the same claim, and clearly acts as a primary basis for rejection in contravention of MPEP 2144.03A&B discussed previously herein.

Accordingly, Applicant submits that the invention of Claim 33 is novel and non-obvious over the cited art, and in condition for allowance.

Claim 40 - By this paper, Applicant has amended Claim 40 to include limitations relating to causing the recited second parallel-load register file to be parallel loaded from a row of said DRAM array, while the parallel-loadable register file is an inactive state. Applicant submits that none of the cited art, including Parady, teaches or suggests such functionality.

Suppose also (as the Examiner suggests) that the claimed "data assembly unit" of the architecture corresponds to Parady's load/store unit 32. Given this mapping, Parady clearly teaches away from the invention of Claim 40 because in Parady, the load/store unit can only access the architectural registers, and cannot access any of the deactivated (aka inactive) register sets.

Furthermore, note that Parady assumes a cache is between the load/store unit 32 and any memory that might be there. Therefore, the load/store unit 32 cannot rightfully be called part of the "data assembly unit" as it is alleged by the Examiner on, *inter alia*, page 41, Par. 71.(iv). "*If the proposed modification or combination of the prior art would change the **principle of operation** of the prior art invention being modified, then the teachings of the references are **not** sufficient to render the claims prima facie obvious.*" MPEP 2143.01 {emphasis added}. Parady teaches away from the claimed invention in at least this regard.

Parady in no way teaches or suggests an embedded DRAM processor nor a method of intelligent caching for such a processor. Applicant traverses the Examiner's use of "Official

Notice" that the use of DRAM would be obvious, because the invention of Claim 40 is specifically designed to provide an intelligent caching interface to slower DRAM. **Applicant requests pursuant to MPEP 2144.03C that the Examiner provide explicit documentation to this effect.**

Accordingly, Applicant submits that the invention of Claim 40 is novel and non-obvious over the cited art, and in condition for allowance.

(vii) Per Par. 72 of the Office Action, Claim 11 was rejected under Section 103(a) over Inagami in view of Hayashi, as well as "Official Notice".

Claim 11 – By this paper, Applicant has added limitations relating to dispatching in parallel a first sequence of instructions and a second sequence of instructions for parallel execution. Support for this amendment is found at, *inter alia*, page 12, lines 10-26 of the specification as filed. None of the cited art teaches or suggests such limitations in combination with the other elements of Claim 11.

Applicant notes that Inagami is a vector processor that executes a single sequence of vector instructions. The parallel-by-element processing of Inagami utilizes a different form of parallelism and pipelining that clearly teaches away from the Applicant's invention. There is no hint or suggestion in Inagami of having the load/store pipelines perform speculative data prefetching for the parallel-by-element processors.

As to the amendments to Claim 11 provided herein, there is no parallel dispatch of separate instructions; Inagami executes only one sequence of vector instructions.

As to combination with Hayashi, note that Hayashi does not perform speculative prefetching of data to avoid delays as in Applicant's invention, but instead has an intricate mechanism to deal with the delays and contentions that occur after-the-fact.

Neither Inagami nor Hayashi teach or suggest an embedded DRAM processor. Applicant traverses the Examiner's use of "Official Notice" that the use of DRAM would be obvious, as previously noted in detail herein. **Applicant requests under MPEP 2144.03C that the Examiner provide explicit documentation to this effect.**

Accordingly, Applicant submits that the invention of Claim 11 is novel and non-obvious over the cited art, and in condition for allowance..

New Claims

By this paper, Applicant adds new Claims 41-43. Applicant submits that Claims 41-43 are fully supported by the specification and drawings as filed, and comprise patentable subject matter.

Other Remarks

Applicant hereby specifically reserves all rights of appeal, as well as the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention and responding to the aforementioned Action, and not for purposes of overcoming art or for patentability. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such claim cancellations or additions.

Furthermore, any remarks made with respect to a particular claim or claims shall be limited to only such claim or claims.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

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